WSGL WEINGARTEN, SCHURGIN, GAGNEBIN & LEBOVICI LLP
Intellectual Property Law
Patents • Trademarks • Copyrights

Ten Post Office Square
Boston, Massachusetts 02109
Tel. 617.542.2290 • Fax. 617.451.0313
www.wsglip.com

FACSIMILE COVER SHEET

DATE: February 24, 2005

TO: Examiner Chat C. Do
TC Art Unit: 2124

Fax No.: (703) 872 9306

FROM: Richard E. Gamache

No. of pages transmitted (including this page): 10

Our File: ADI-005XX

Time:

Your Ref:
Application No. 09/630,258
Filed Date: August 1, 2000
Confirmation No.: 7200

Sent by: Paula Derby

A confirmation copy of this transmission will not be mailed unless the following is checked: [ ]

MESSAGE

PLEASE DELIVER DIRECTLY TO:
EXAMINER CHAT C. DO, Tel. (571) 272-3721
TC ART UNIT NO: 2124

FOR ENTRY

Enclosed for filing please find a Request for Telephonic Interview.

The Commissioner is hereby authorized to Charge Deposit Account No. 23-0804 for any additional filing fees associated with this communication or credit any overpayment.

Attorney for Applicant: Richard E. Gamache
Registration No. 39,196

REG/pjd/317856

Application No.: 09/630,253
Filed: August 1, 2000
TC Art Unit: 2124
Confirmation No.: 7200

Rev 12/04

WEINGARTEN, SCHURGIN, GAGNEBIN & LEBOVICI LLP
Ten Post Office Square
Boston, Massachusetts 02109
Telephone: (617) 542-2290
Telecopier: (617) 451-0313

Date: February 24, 2005

Via Facsimile
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney
Docket No.: ADI-005XX

Sir:

In re application of: Marc Hoffman et al.

Entitled: A METHOD FOR EFFICIENTLY COMPUTING A FAST FOURIER TRANSFORM

Transmitted herewith is a Request for Telephonic Interview for the above-identified application. The following checked items are applicable:

[ ] This is a Request for Continued Examination under §1.114; authorization is provided herewith to charge Deposit Account No. 23-0804 for the cost of same ($_____) per §1.17(e).
[ ] Enter the unentered amendment previously filed on _____ per §1.116.

[ ] A Petition for Extension of Time for ___ month is hereby made under §1.136(a); authorization is provided herewith to charge Deposit Account No. 23-0804 for the cost of same ( ) per §1.17.

[X] In the event a Petition for Extension of Time is required by this paper and not otherwise provided, such Petition is hereby made and authorization is provided herewith to charge Deposit Account No. 23-0804 for the cost of such extension.

[ ] Other:

CLAIMS AFTER AMENDMENT:	MINUS PRIOR PAID CLAIMS:	EQUALS PRESENT EXTRA CLAIMS:	RATE:	ADDITIONAL FEE:
Independent	3 - 3	= 0	x $200.00 =	0
Total	8 - 8	= 0	x $ 50.00 =	0
[ ] Multiple Dependent Claims (1st presentation)			+ $360.00 =	0
SUBTOTAL ADDITIONAL FEE				0
Small Entity filing, divide by 2. Small Entity status must be asserted.				0
TOTAL ADDITIONAL FEE				0

[X] No additional fee. [ ] The fee has been calculated above; authorization is provided herewith to charge Deposit Account No. 23-0804 ($_____) for the cost of same.

[X] **The Commissioner is hereby authorized to charge payment of any additional filing fees under §1.16 associated with this communication or credit any overpayment to Deposit Account No. 23-0804.**

I hereby certify that this correspondence is being sent via facsimile to Examiner Chat C. Do, TC Art Unit 2124, Fax No. (703) 872 9306, on 2/24/05.

Richard E. Gamache

Attorney of Record: Richard E. Gamache
Registration No.: 39,196

REG/pjd/317855

PATENT

Rev 12/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application	:	Marc Hoffman, et al.
Application No.	:	09/630,258
Filed	:	August 1, 2000
Confirmation No.	:	7200
For	:	A METHOD FOR EFFICIENTLY COMPUTING A FAST FOURIER TRANSFORM
Examiner	:	Chat C. Do
Attorney's Docket	:	ADI-005XX

TC Art Unit: 2124

* *

I hereby certify that this correspondence is being sent via facsimile to Examiner Chat C. Do, TC Art Unit 2124 Fax No. 703-872-9306, on 2/24/05.

By Richard E. Gamache
Richard E. Gamache
Registration No. 39,196
Attorney for Applicants

* *

REQUEST FOR TELEPHONIC INTERVIEW

Via Facsimile
Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a request for a telephonic interview to afford the Applicants an opportunity to discuss the Examiner's rejections of claims 1-8, as indicated in the official action dated November 17, 2004 in the above-referenced application. Via a discussion of the following arguments for the patentability of claims 1-8, the Applicants seek to clarify the outstanding issues in the above-

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

referenced application, thereby advancing the instant application toward allowance.

Specifically, base claim 1 recites a method of computing a fast Fourier transform in a plurality of computation stages, including the steps of

(a) receiving N time-ordered first data values;

(b) sequentially storing in a first memory each of said N time-ordered first data values in the time-order;

(c) storing in a second memory a plurality of twiddle factors in a bit reversed order;

(d) reading a predetermined number R of input butterfly data values of said N first data values, wherein said predetermined number R of input butterfly data values are separated by N/R first data values in said N time-ordered first data values;

(e) performing a radix R butterfly calculation on said predetermined number R of input butterfly data values using at least one of the plurality of twiddle factors stored in the second memory to generate R output butterfly data values;

(f) storing said R output butterfly data values in *sequential memory locations of a third memory*; and

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

Application No. 09/630,258
Filed: August 1, 2000
TC Art Unit: 2124
Confirmation No.: 7200

(g) performing said steps (c) - (f) N/R x 2 times, wherein the predetermined number R is the same predetermined number each time the steps (d) - (f) are performed,

wherein said reading step (d) includes reading the R output butterfly data values from said third memory,

wherein the memory store operation performed in said storing step (f) has *a unity stride*, thereby allowing R output butterfly data values to be read from *contiguous memory locations* each time the R output butterfly data values are read from said third memory, and

wherein said steps (a) - (g) are performed in *each one* of the plurality of computation stages.

The Examiner has rejected claims 1-8 under 35 U.S.C. 102(e) as being anticipated by Kiamilev *et al.* (USP 5,951,627). The Applicants respectfully submit, however, that the Kiamilev reference does not disclose each and every element/step of claims 1-8. For example, the Kiamilev reference does not disclose the method of claim 1, including storing R output butterfly data values in sequential locations of a third memory such that the memory store operation (step (f)) has a unity stride, thereby allowing the R output butterfly data values to be read from *contiguous locations* of the third memory *each time* the R output

WEISGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

butterfly data values are read from the memory, and the steps (a) - (g) are performed in *each one* of a plurality of computation stages.

This deficiency of the Kiamilev reference is depicted in Figs. 2 and 6 of that reference. As shown in Fig. 2 of Kiamilev *et al.*, a 16-point FFT processor array includes stages 1-4, in which each stage provides 16 output butterfly data values. Although stage 4 is depicted as providing its 16 output butterfly data values to sequential locations 0-15, the Applicants respectfully submit that stages 1-3 do not provide their 16 butterfly data value outputs to sequential locations within the FFT processor array. For example, with respect to stage 1 (see Fig. 2 of Kiamilev *et al.*), a first butterfly processor having inputs x(0) and x(8) provides its two outputs x(0) and x(1) to non-sequential locations, *i.e.*, a 0^{th} location and a 2^{nd} location, in the FFT processor array; a second butterfly processor having inputs x(1) and x(9) provides its two outputs x(2) and x(3) to non-sequential locations, *i.e.*, a 4^{th} location and a 6^{th} location, in the FFT processor array; a third butterfly processor having inputs x(2) and x(10) provides its two outputs x(4) and x(5) to non-sequential locations, *i.e.*, an 8^{th} location and a 10^{th} location, in the FFT processor array, *etc.* Because the outputs of

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

the butterfly processors in each stage 1-3 are not provided to sequential locations in the FFT processor array, the memory store operations at the output of each stage 1-3 do not have a unity stride, as recited in claim 1. To assure that the outputs of the butterfly processors in stage 4 are provided to sequential locations in the FFT processor array, a re-shuffling of its outputs x(0)-x(15) is required, as depicted in Fig. 2 of Kiamilev *et al.* This clearly indicates that the same processing steps are not performed in each one of the stages 1-4, as recited in claim 1.

As shown in Fig. 6 of Kiamilev *et al.*, a multi-stage FFT calculation system employs multiple virtual memory banks 0-3, in which each bank 0-3 is subdivided into four physical blocks of storage. Although the Kiamilev reference indicates that data from a previous stage can be read directly into a current stage with no transformations (see column 6, lines 39-40, of Kiamilev *et al.*), the output butterfly data values of each stage are not provided to sequential locations of a memory, and therefore the output data values are not read from contiguous memory locations each time the outputs are read from the memory, as recited in claim 1. Instead, output data values are first read from the same address of banks 0 and 2. Next, banks 1 and 3 are accessed at the same address. The

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

accessing of the memory banks 0-3 then alternates between the even-numbered and odd-numbered banks to assure that each butterfly processor gets data inputs that are N/2 points apart from each other (see column 6, lines 15-21, of Kiamilev *et al.*).

In contrast, the method of claim 1 recites the step of storing R output butterfly data values in sequential memory locations of a memory such that the memory store operation has a unity stride, thereby allowing the R output butterfly data values to be read from contiguous memory locations of the memory each time the R output butterfly data values are read from the memory. Significantly, no alternation between even-numbered and odd-numbered memory banks is required in the method of claim 1 to assure that each butterfly processor receives data inputs that are N/2 points apart from each other. As a result, the method of claim 1 can be used to compute an FFT in a manner that both reduces the number of required iterations and simplifies the calculation of the storage locations of the output data values from each memory stage (see page 6, lines 17-21, of the application).

This is illustrated in Fig. 6 of the instant application, which depicts an 8-point FFT processor including 3 stages, each stage providing 8 output butterfly data values. Unlike the FFT

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

Application No. 09/630,258
Filed: August 1, 2000
TC Art Unit: 2124
Confirmation No.: 7200

processor array disclosed in Fig. 2 of the Kiamilev reference, each stage of the FFT processor depicted in Fig. 6 of the application provides its 8 butterfly data value outputs to sequential locations in the FFT processor. For example, a first butterfly processor of the first stage of Fig. 6 has inputs x(0) and x(4), and provides its two outputs x(0) and x(1) to sequential locations, *i.e.*, a 0^{th} location and a 1^{st} location, in the FFT processor. Similarly, a second butterfly processor of the first stage having inputs x(1) and x(5) provides its two outputs x(2) and x(3) to sequential locations, *i.e.*, a 2^{nd} location and a 3^{rd} location, in the FFT processor. The remaining butterfly processors of the first stage also provide their outputs to sequential locations 4-7 in the FFT processor, as do the butterfly processors contained in each one of the second and third stages of the FFT processor.

Because the Kiamilev reference neither teaches nor suggests that R output butterfly data values are stored in sequential memory locations of a memory such that the memory store operation (step (f) of claim 1) has a unity stride, thereby allowing the R output data values to be read from contiguous memory locations of the memory each time the R output data values are read from the memory, and that steps (a) – (g) of claim 1 are performed in each

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

Application No. 09/630,258
Filed: August 1, 2000
TC Art Unit: 2124
Confirmation No.: 7200

one of the FFT computation stages, as recited in claim 1, the Kiamilev reference does not anticipate claim 1. Similar arguments can be made in favor of the patentability of base claims 5 and 8.

The undersigned Attorney will telephone the Examiner to discuss the possible scheduling of the requested telephonic interview.

Respectfully submitted,

MARC HOFFMAN, ET AL.

By: Richard E. Gamache

Richard E. Gamache
Registration No. 39,196
Attorney for Applicants

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
Ten Post Office Square
Boston, MA 02109
Telephone: (617) 542-2290
Telecopier: (617) 451-0313

REG/pjd/307428